REMARKS

Claims 21 and 26 have been amended, and claims 1-20, 25 and 30 have been cancelled. Claims 21-24 and 26-29 are pending in the application.

A Revocation and Power of Attorney by Assignee and Exclusion of Inventors Under 37. C.F.R. 3.71 will be filed in due course.

In view of the above amendments and the following remarks, the applicants respectfully request favorable reconsideration and allowance of the application.

The sections set forth below are presented in the same order as that of the Action for ease of reference.

The Drawings

The drawings were objected to because of an error in Fig. 3. In particular, on page 7, lines 3-6 of the application, the circuit of Fig. 3 is described as being configured to produce a positive portion of the unipolar PWM output voltage signal, wherein the switch SW22 is maintained in a conducting state while switch SW21 is maintained in a non-conducting state. However, Fig. 3 as originally filed does not show such an arrangement. Thus, enclosed herewith for the Examiners' approval is a proposed correction of Fig. 3 that shows the correct switch arrangement with SW21 in a non-conducting state and SW22 in a conducting state. A second copy of Fig. 3 marked in red ink has also been enclosed to show the changes. Support for this amendment can be found on page 7, lines 3-6 of the application. No new matter has been added.

In view of the amendment to Fig. 3, the applicant respectfully requests withdrawal of the objection to the drawings.

Claim Rejections under 35 U.S.C. 102(b)

Claims 21-30 were rejected for being anticipated by Otsuka, U.S. Patent No. 4,325,112("Otsuka").

Independent claim 21 has been amended, and now pertains to an apparatus to generate a pulse width modulated voltage signal that includes a DC voltage source, first and second switching circuits, an output, and a microprocessor. The microprocessor is electrically coupled to the first and second switching circuits, wherein the microprocessor generates control signals according to a selected pulse width modulation scheme to control the timing and operation of the first and second switching circuits. Similarly, independent method claim 26, directed to a method of generating a pulse width modulated voltage signal,

has been amended to include the step of generating control signals with a processor according to a selected pulse width modulation scheme to control the timing and operation of the first and second switching circuits. Claim 26 has also been amended to make it clear that the step of maintaining the third switch in a conduction state while maintaining said fourth switch in a non-conducting state occurs according to the control signals so as to establish a first polarity of an output signal, and that the first and second switches are switched at a selected modulation frequency, and then maintaining the second switch in a conducting state while maintaining the first switch in a non-conducting state according to the control signals so as to establish a second polarity of said output signal. Support for these changes can be found, for example, in former claims 25 and 30, and in the specification on page 6, lines 28-30 and in Fig. 9. No new matter has been added. Independent claims 21 and 26 thus now recite utilizing a microprocessor to generate control signals according to a selected PWM scheme to control the timing and operation of the first and second switching circuits.

In contrast, Otsuka is directed to a counter-controlled pulse width modulated (PWM) inverter having a main circuit with switching means, and a control circuit for controlling the on-off operation of the switching means (see Fig. 3 of Otsuka). In particular, the on-off operation of the switching means of the main circuit obtains a predetermined voltage-time-integration value according to the electrical angle θ of the output voltage waveform of the inverter. That is, the device has PWM control means for comparing voltage-time-integration values (see col. 3, lines 41-50 and claim 1 of Otsuka). Otsuka recites that a primary objective of his invention is to provide an improved voltage source inverter in which the control circuit is simple (see col. 2, lines 6-8). To that end, Otsuka teaches and claims a control circuit that requires a function generator to output a first signal proportional to the voltage-time-integration value of an AC voltage waveform in correspondence with an electrical angle of that AC voltage waveform, a time counter for outputting a second signal representative of the integrated time of the ON period of the switching means, a comparator, and a logic circuit for controlling the on-off operation of the switching means in response to the output of the comparator (see col. 2, lines 19-30 and claim 1, lines 16-29 of Otsuka). The applicants respectfully assert that at the time Otsuka's invention was made, a microprocessor would not be considered or utilized as such devices were expensive and viewed as overly complex. Accordingly, Otsuka does not suggest or teach to utilize a microprocessor as claimed in the present application. Thus, independent claims 21 and 26 are not anticipated.

In view of the above remarks, the applicant respectfully requests withdrawal of the 35 U.S.C. 102(b) rejections of independent claims 21 and 26. In addition, claims 22-24 and 27-29 all directly depend on either claim 21 or claim 26, and thus should also be allowable for at least the same reasons.

In view of the amendments and remarks made herein, the applicants respectfully submit that the entire application is in condition for allowance, early notice of which would be appreciated. Should the Examiner not agree that all pending claims are allowable, then a personal or telephonic interview is respectfully requested to discuss any remaining issues and expedite the eventual allowance of these claims

Respectfully submitted,

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Amendments to the Drawings:

The attached sheet of drawings include changes to Fig. 3 on sheet 2 of 7. Also enclosed is a copy of sheet 2 of 7 containing Fig. 3 marked in red ink to show where the changes have been made.

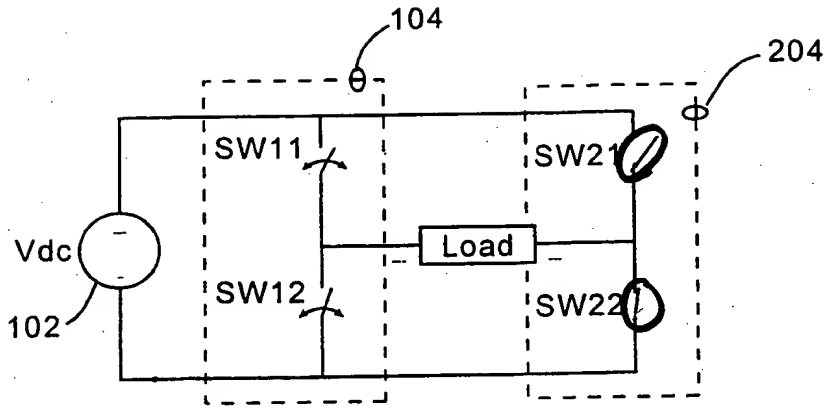
104
204
SW11
SW21
Vdc
Load
SW12
SW22
102

FIG. 3

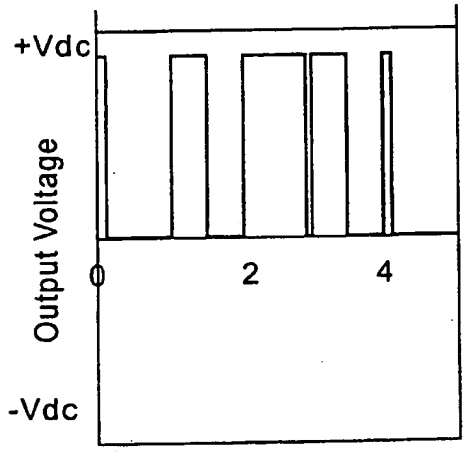
+Vdc
Output Voltage
0
2
4
-Vdc

FIG. 4